FIG. 1A

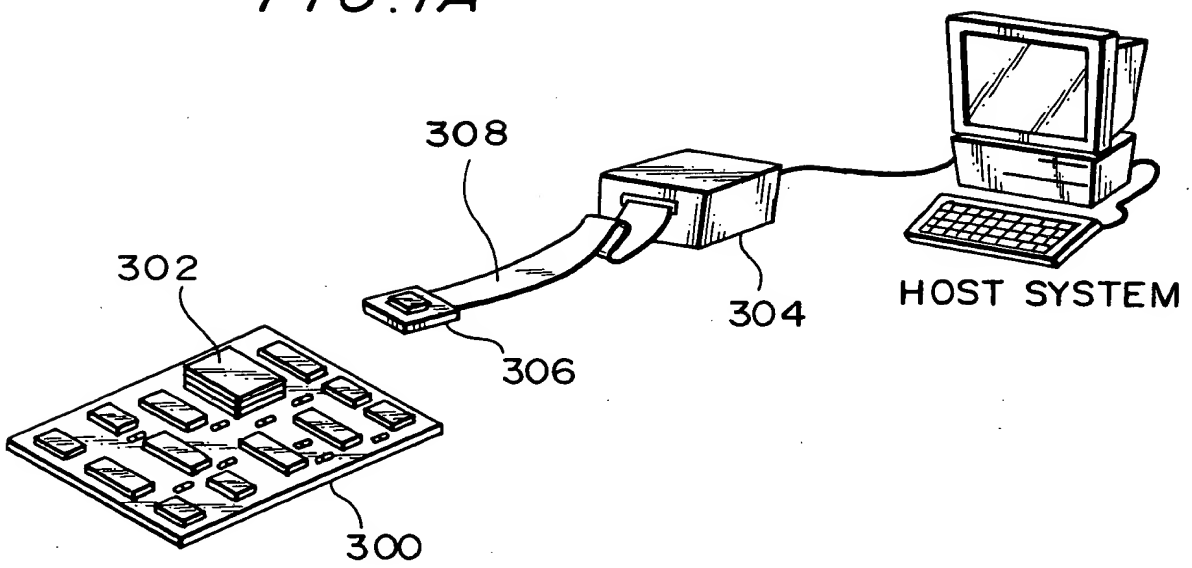

308
302
304
HOST SYSTEM
306
300

FIG. 1B

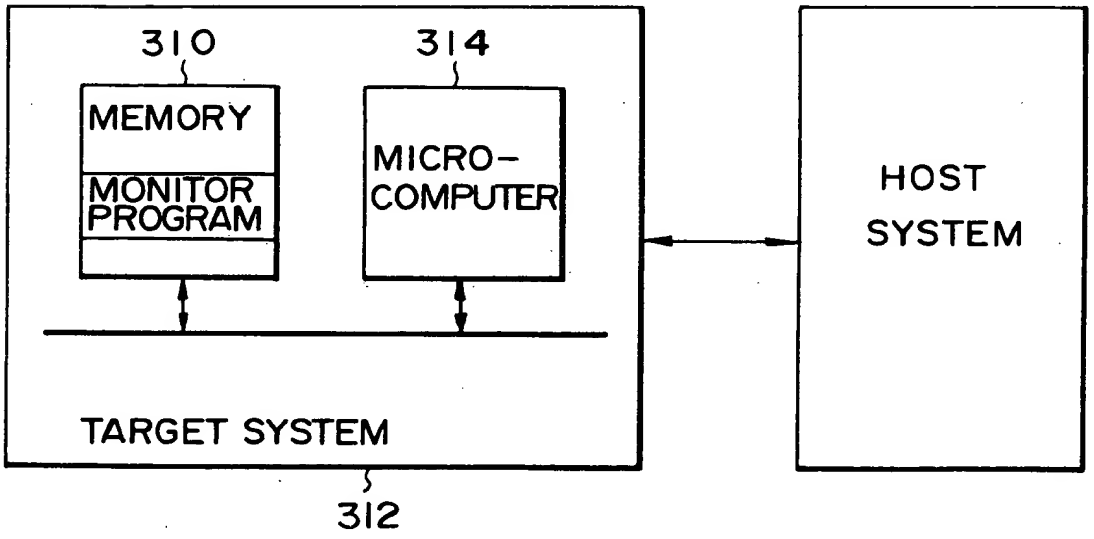

310
314
MEMORY
MONITOR PROGRAM
MICRO-COMPUTER
HOST SYSTEM
TARGET SYSTEM
312

FIG. 2

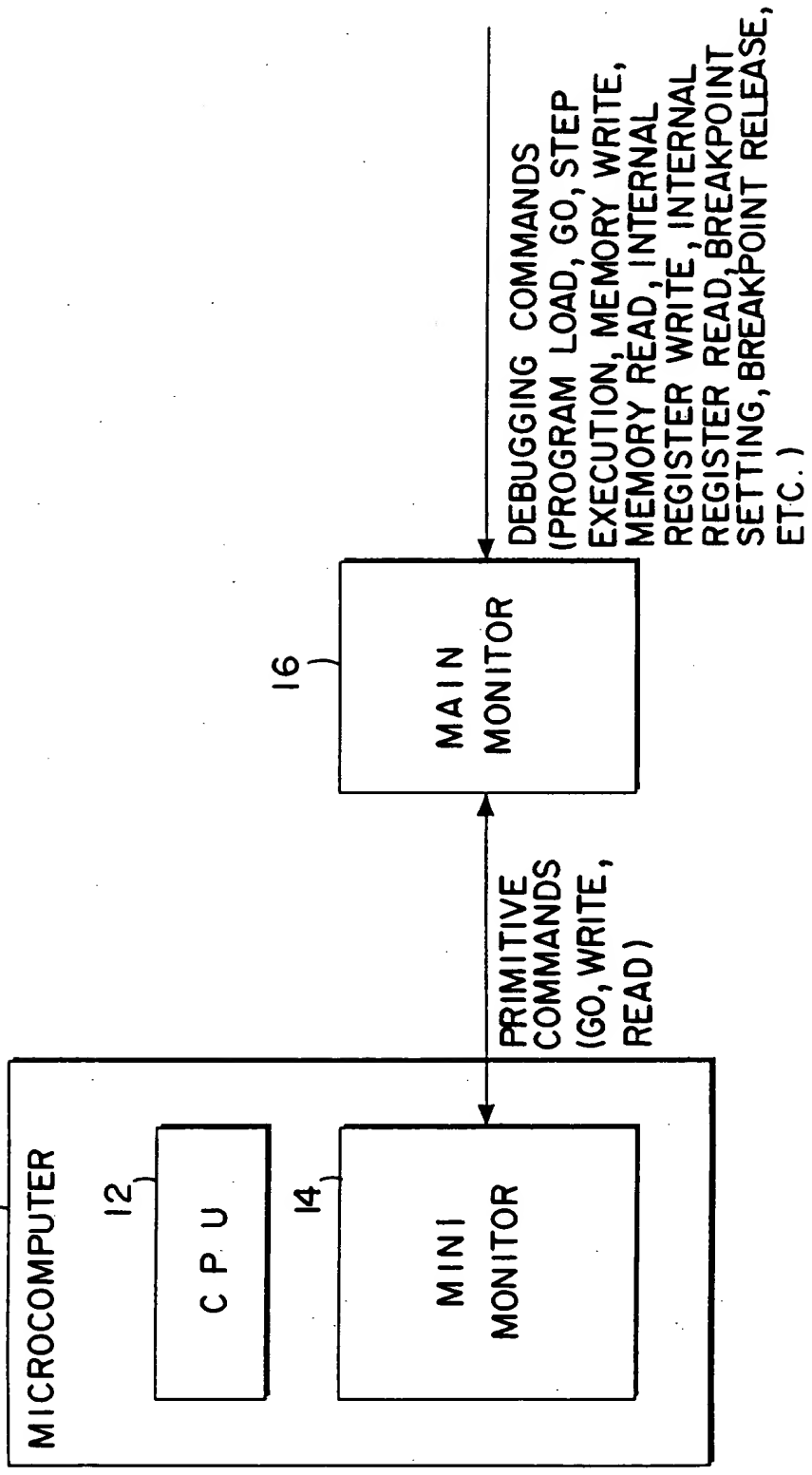

MICROCOMPUTER
10
CPU
12
MINI MONITOR
14
MAIN MONITOR
16
PRIMITIVE COMMANDS (GO, WRITE, READ)
DEBUGGING COMMANDS (PROGRAM LOAD, GO, STEP EXECUTION, MEMORY WRITE, MEMORY READ, INTERNAL REGISTER WRITE, INTERNAL REGISTER READ, BREAKPOINT SETTING, BREAKPOINT RELEASE, ETC.)

FIG. 3

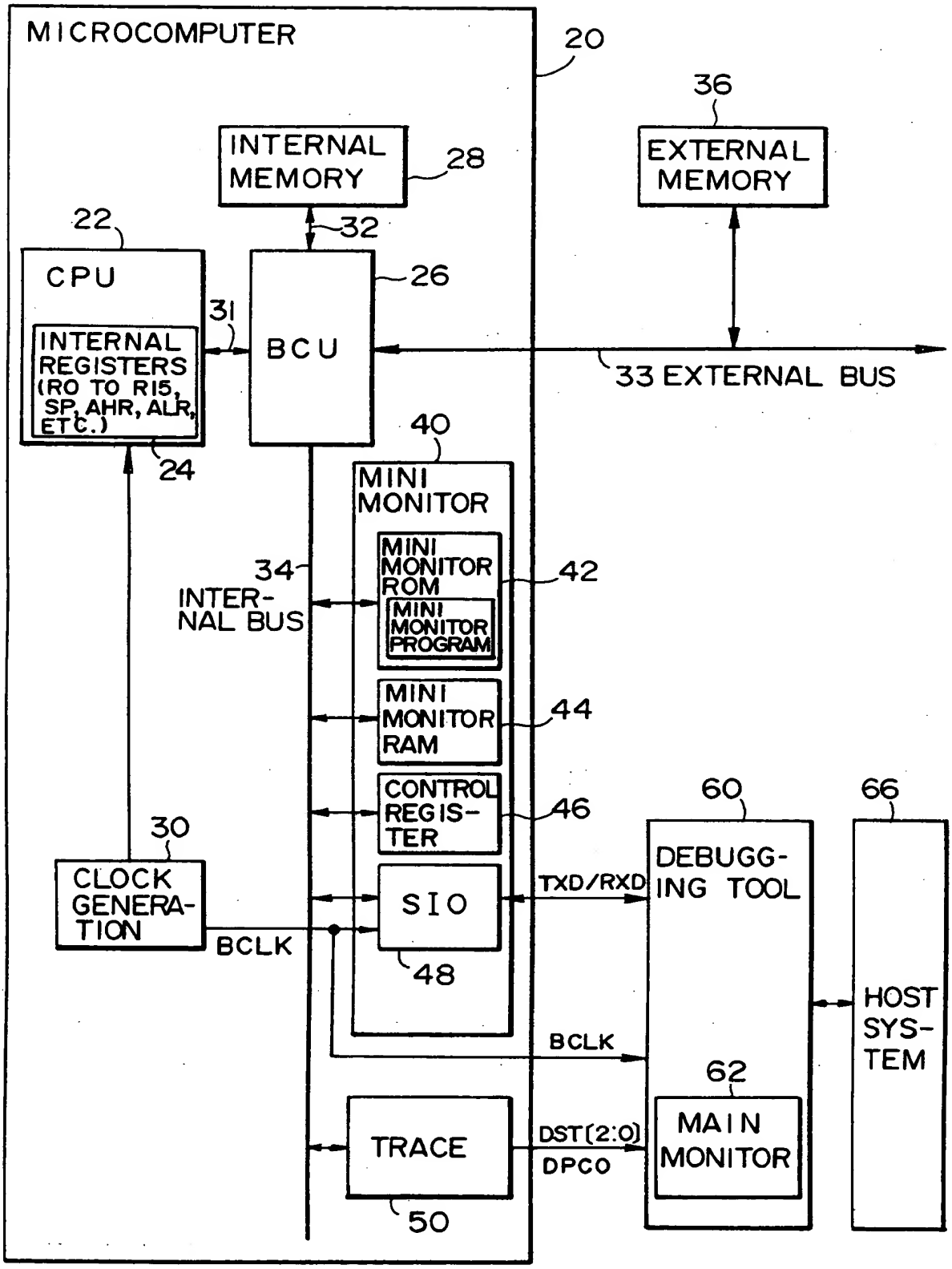
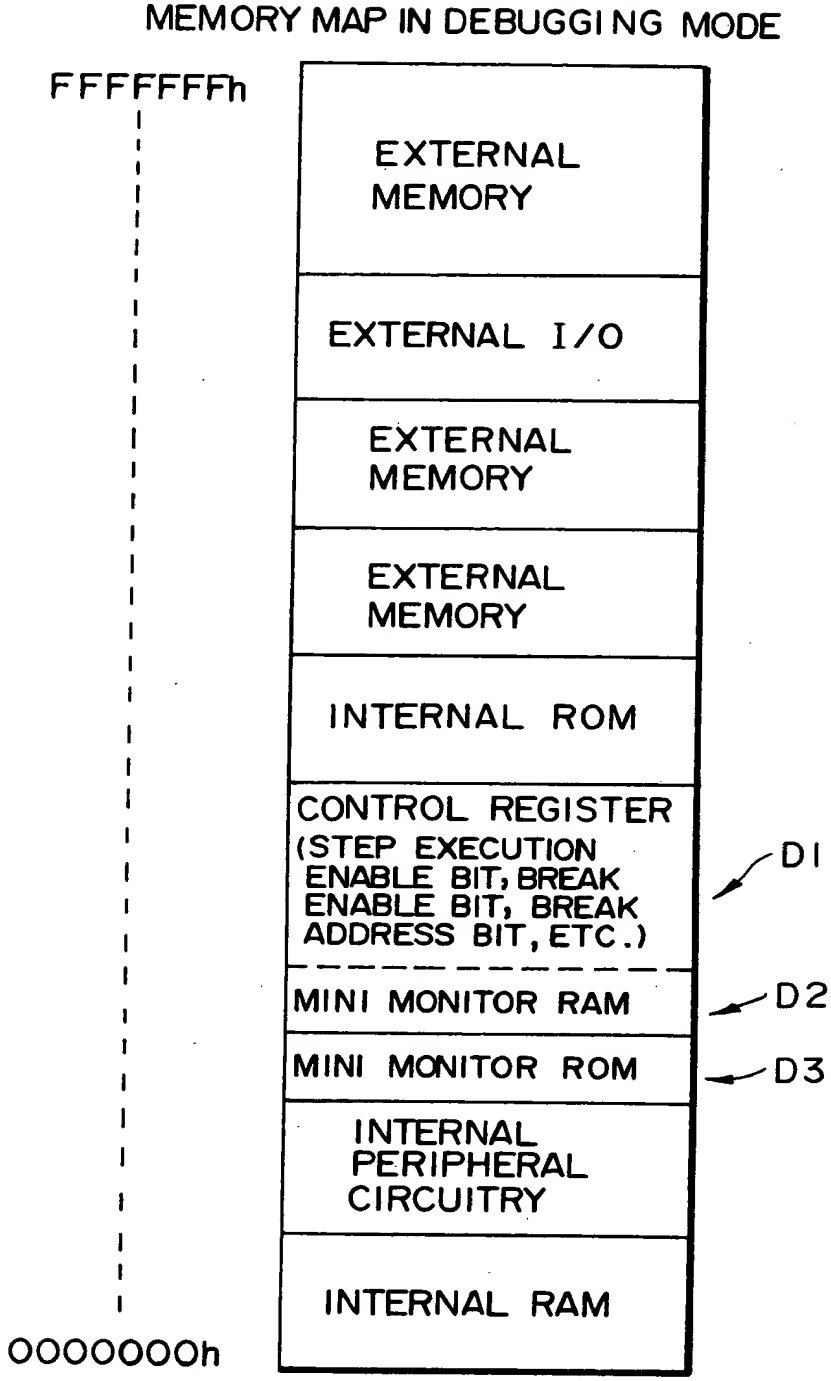

MICROCOMPUTER
20
36
INTERNAL MEMORY
28
EXTERNAL MEMORY
22
32
CPU
26
31
INTERNAL REGISTERS (R0 TO R15, SP, AHR, ALR, ETC.)
BCU
33 EXTERNAL BUS
40
MINI MONITOR
34
INTER-NAL BUS
MINI MONITOR ROM
42
MINI MONITOR PROGRAM
MINI MONITOR RAM
44
CONTROL REGIS-TER
46
60
66
30
CLOCK GENERA-TION
BCLK
SIO
TXD/RXD
DEBUGG-ING TOOL
48
HOST SYS-TEM
BCLK
62
TRACE
DST(2:0)
DPCO
MAIN MONITOR
50

FIG. 4


MEMORY MAP IN DEBUGGING MODE
FFFFFFFh
EXTERNAL MEMORY
EXTERNAL I/O
EXTERNAL MEMORY
EXTERNAL MEMORY
INTERNAL ROM
CONTROL REGISTER (STEP EXECUTION ENABLE BIT, BREAK ENABLE BIT, BREAK ADDRESS BIT, ETC.)
D1
MINI MONITOR RAM
D2
MINI MONITOR ROM
D3
INTERNAL PERIPHERAL CIRCUITRY
INTERNAL RAM
0000000h

POSTED: 2/9/2000

FIG. 5A

PROGRAM LOAD

(80010h, 12 BYTES, ADD---, SUB---
AND---, OR---, XOR---, LD.W---) ⇒ WRITE(80010h, ADD---, SUB---)
+WRITE(80014h, ADD---, OR---)
+WRITE(80018h, XOR---, LD.W---)

FIG. 5B

STEP EXECUTION ⇒ WRITE TO STEP EXECUTION ENABLE BIT OF CONTROL REGISTER
+GO

FIG. 5C

INTERNAL REGISTER READ ⇒ READ MONITOR RAM ON MEMORY MAP

FIG. 5D

BREAKPOINT SETTING ⇒ WRITE TO BREAK ENABLE BIT AND BREAK ADDRESS BIT OF CONTROL REGISTER

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FIG. 6

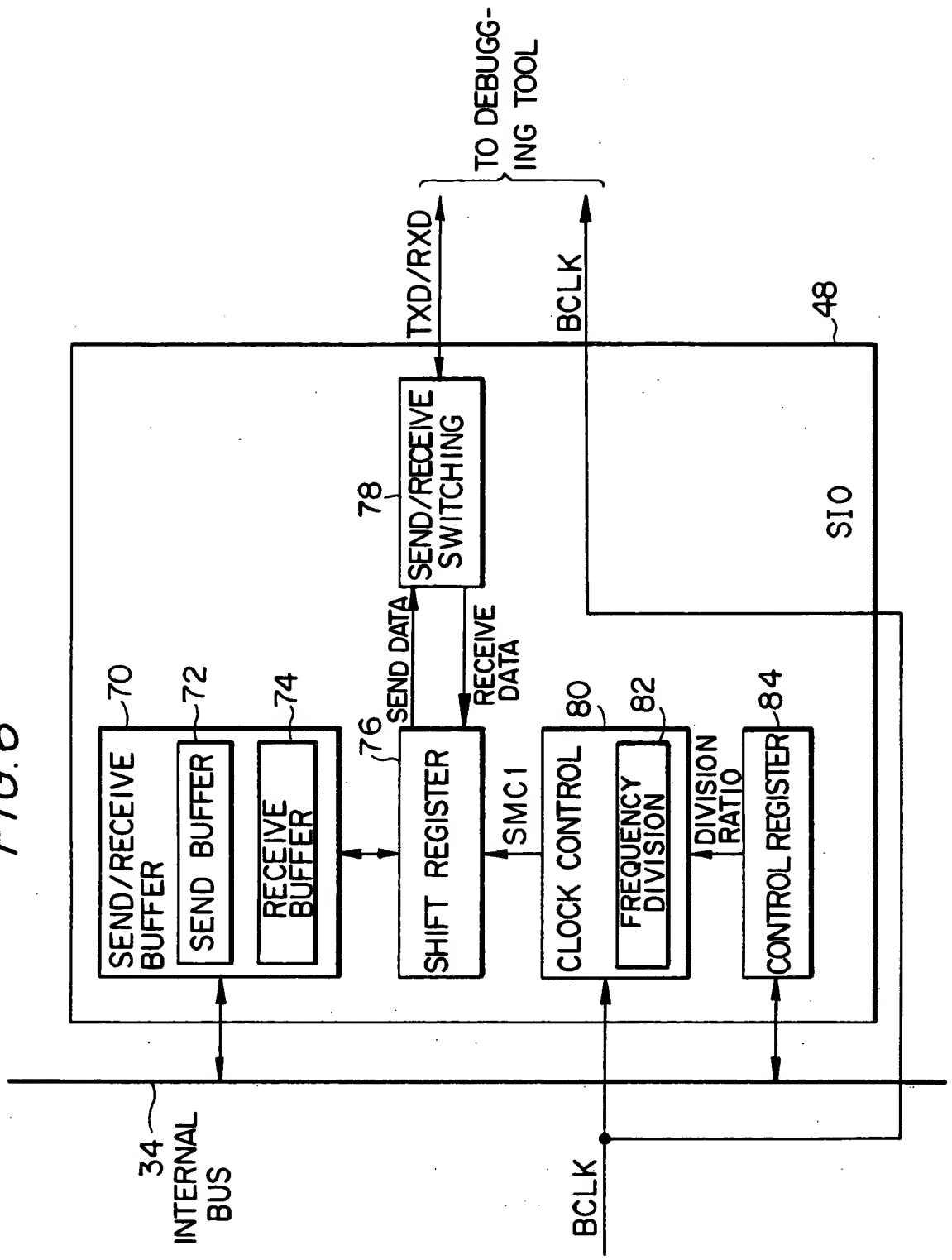
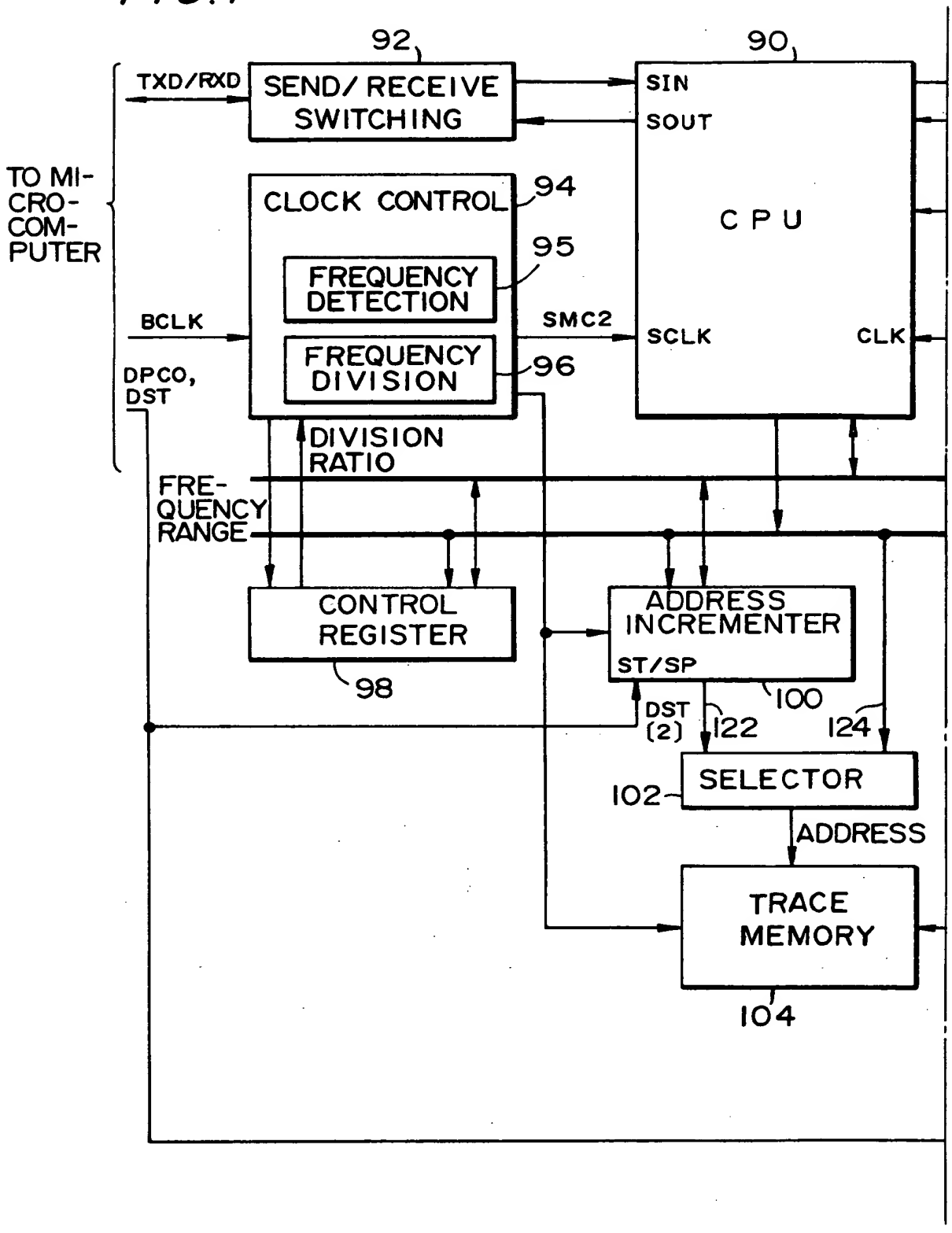

TO DEBUGG-ING TOOL
TXD/RXD
BCLK
48
SIO
78
SEND/RECEIVE SWITCHING
SEND DATA
RECEIVE DATA
70
72
74
76
80
82
84
SEND/RECEIVE BUFFER
SEND BUFFER
RECEIVE BUFFER
SHIFT REGISTER
SMC1
CLOCK CONTROL
FREQUENCY DIVISION
DIVISION RATIO
CONTROL REGISTER
34
INTERNAL BUS
BCLK

FIG. 7


92
90
TXD/RXD
SEND/ RECEIVE SWITCHING
SIN
SOUT
TO MI-CRO-COM-PUTER
CLOCK CONTROL
94
C P U
95
FREQUENCY DETECTION
BCLK
SMC2
SCLK
CLK
FREQUENCY DIVISION
96
DPCO, DST
DIVISION RATIO
FRE-QUENCY RANGE
CONTROL REGISTER
98
ADDRESS INCREMENTER
ST/SP
100
DST (2)
122
124
SELECTOR
102
ADDRESS
TRACE MEMORY
104

7/26 (con't)

FIG. 7 (con't)

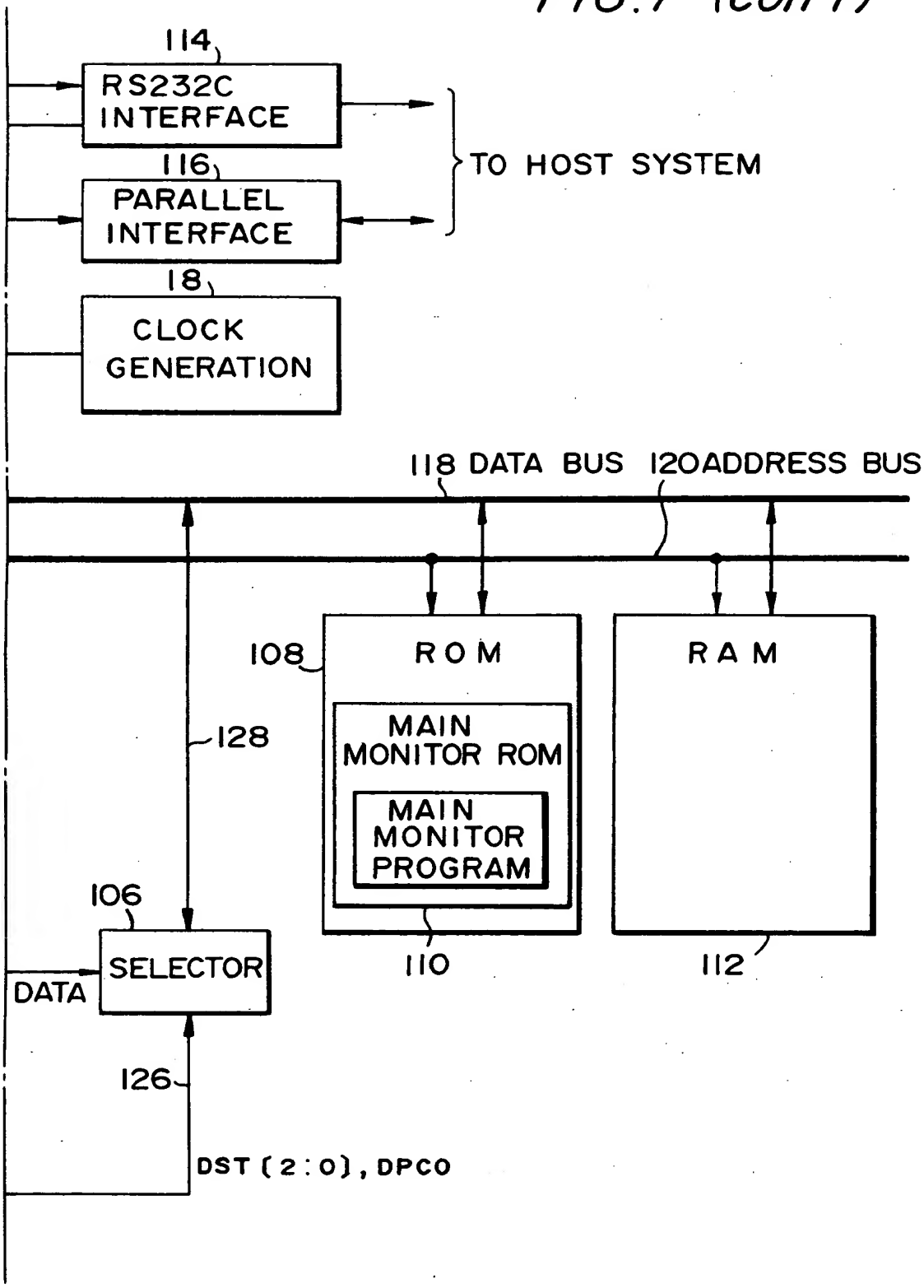


FIG. 8A

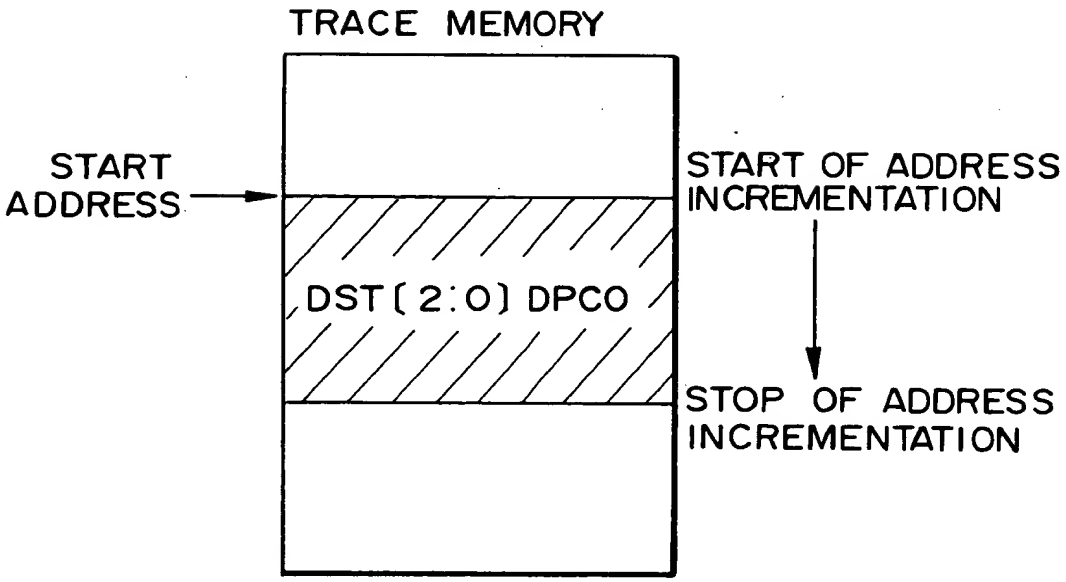

TRACE MEMORY
START ADDRESS
START OF ADDRESS INCREMENTATION
DST[2:0] DPCO
STOP OF ADDRESS INCREMENTATION

FIG. 8B

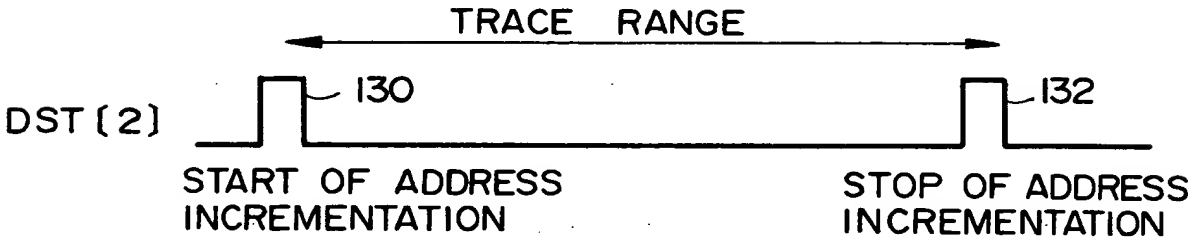

TRACE RANGE
DST[2]
130
132
START OF ADDRESS INCREMENTATION
STOP OF ADDRESS INCREMENTATION

FIG. 9A

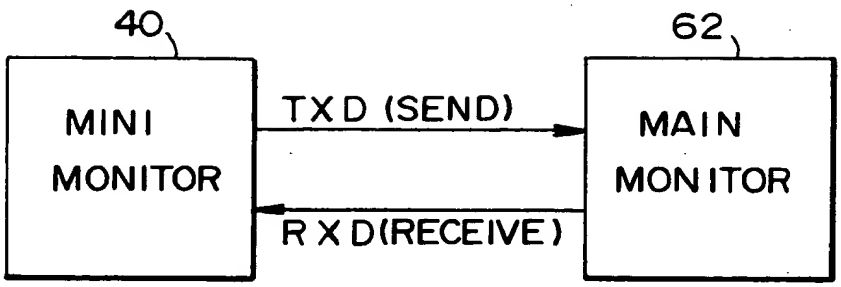


FIG. 9B

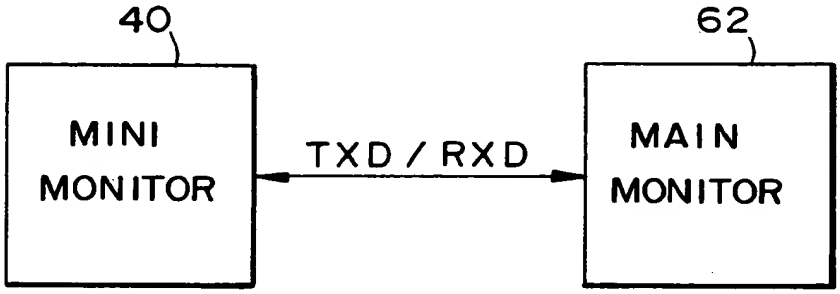


FIG. 9C

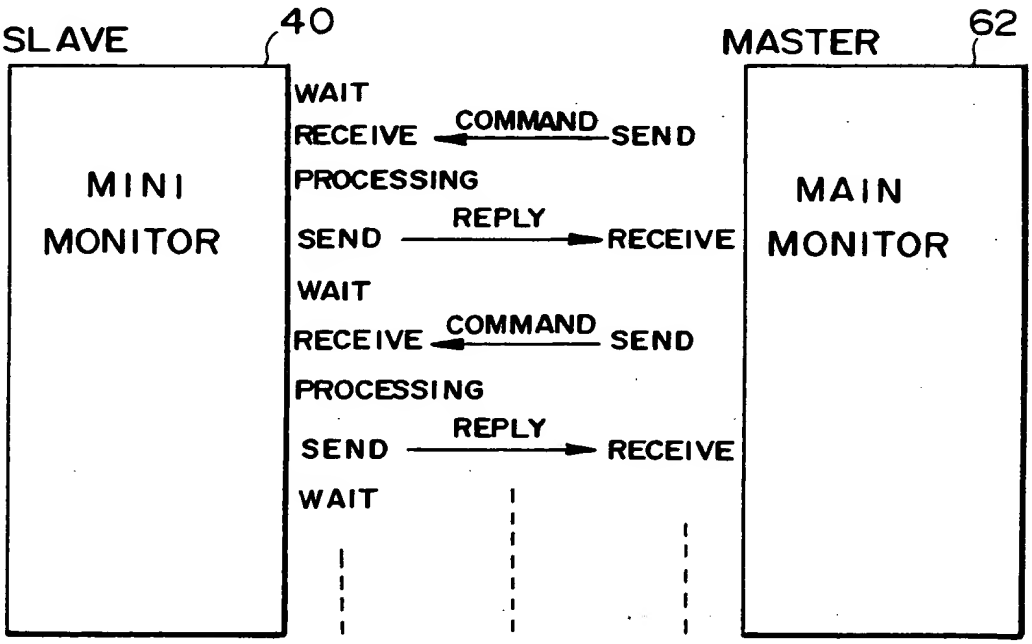


FIG. 10A DATA FORMAT

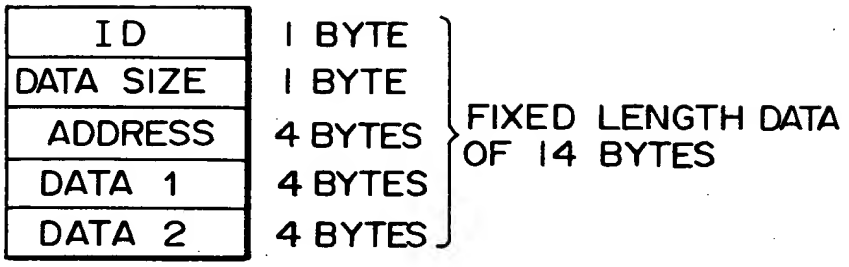


FIG. 10B GO COMMAND

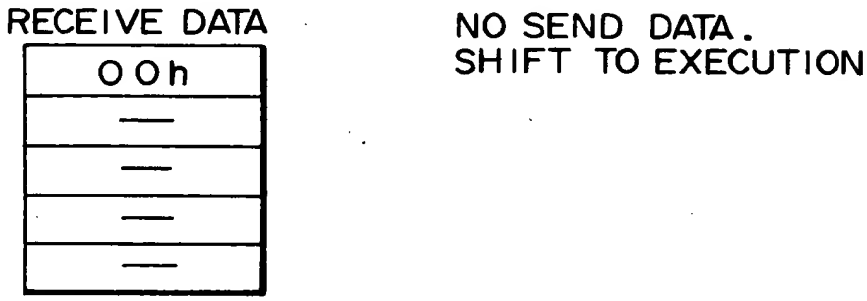


FIG. 10C WRITE COMMAND

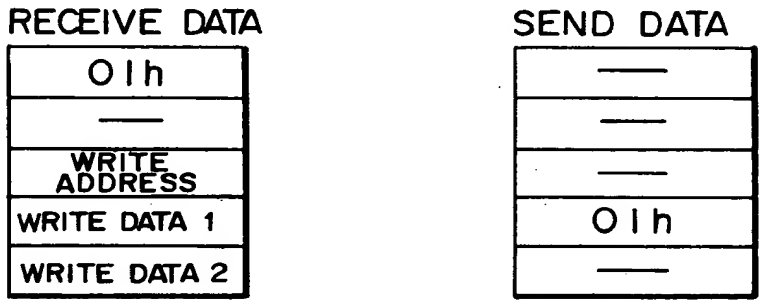


FIG. 10D READ COMMAND

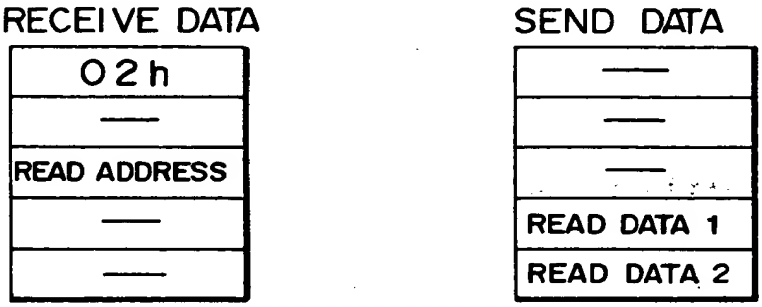


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FIG. 11A

EXTERNAL ROUTINE JUMP COMMAND

RECEIVE DATA		SEND DATA	
03h		—	
18h	(DATA FOR CHECKING MALFUNCTION)	—	
%R12	(ROUTINE ADDRESS)	—	
%R13	(WRITE DATA)	%R10	(RETURN VALUE. WHEN IT IS ZERO, PROGRAM NORMALLY TERMINATES)
%R14	(DATA ADDRESS)	—	

FIG. 11B

DATA FILL COMMAND

RECEIVE DATA	SEND DATA
04h	—
1,2,4	—
START ADDRESS	—
FILL NUMBER	04h
FILL PATTERN	—

FIG. 12A

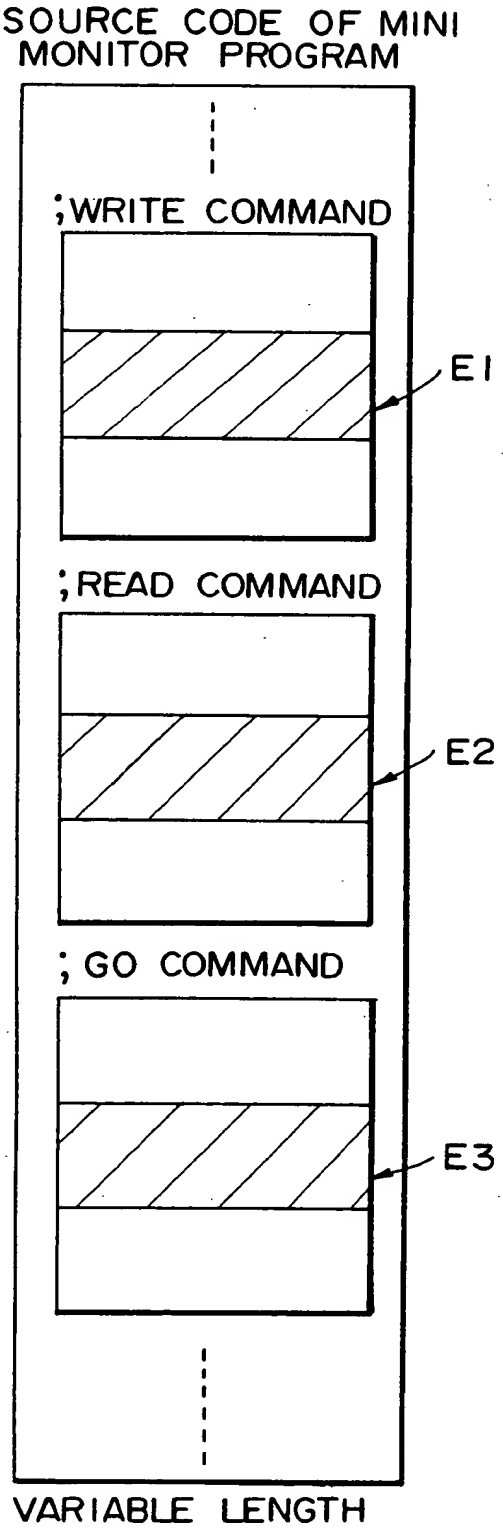


FIG. 12B

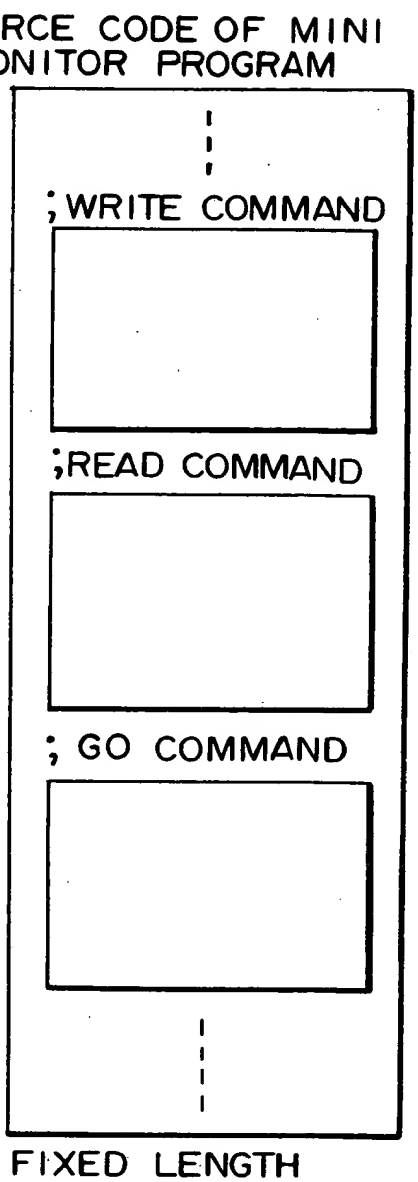


FIG. 13A

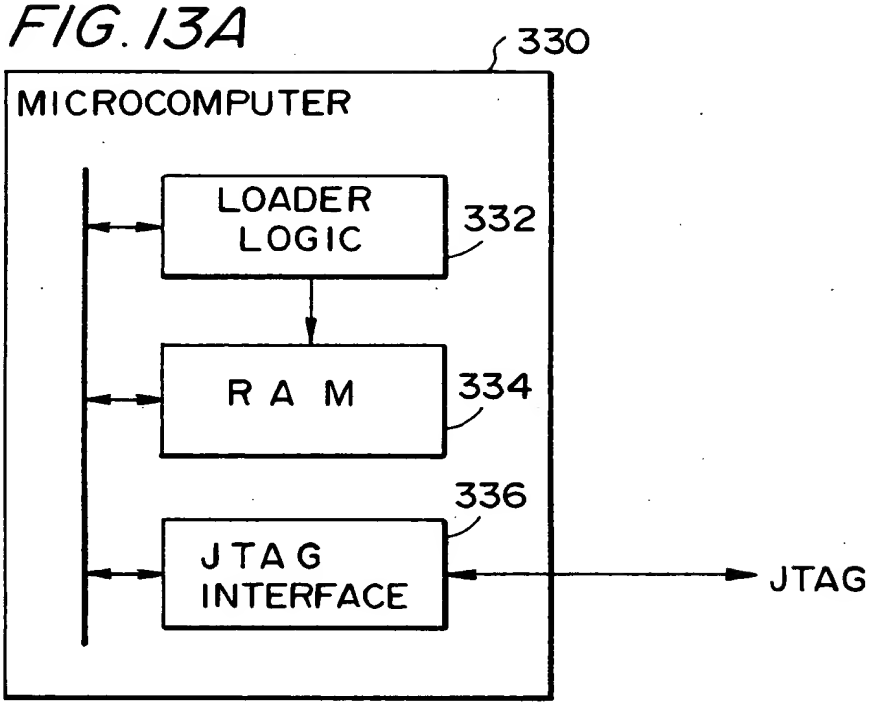


FIG. 13B

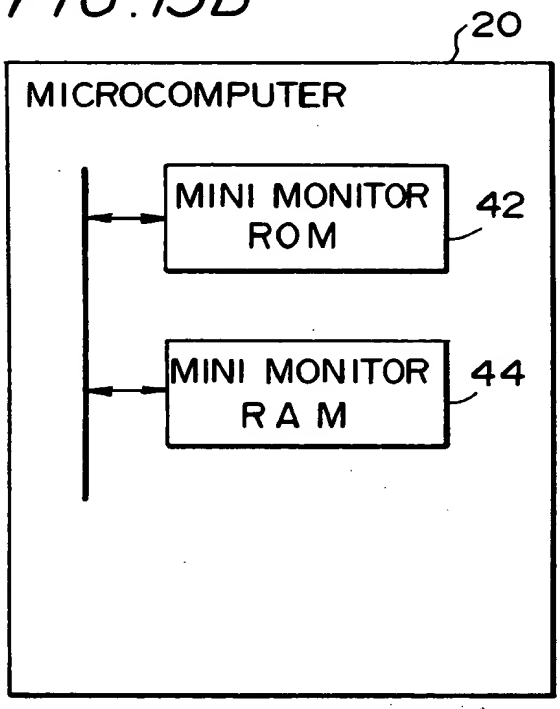


FIG. 14A

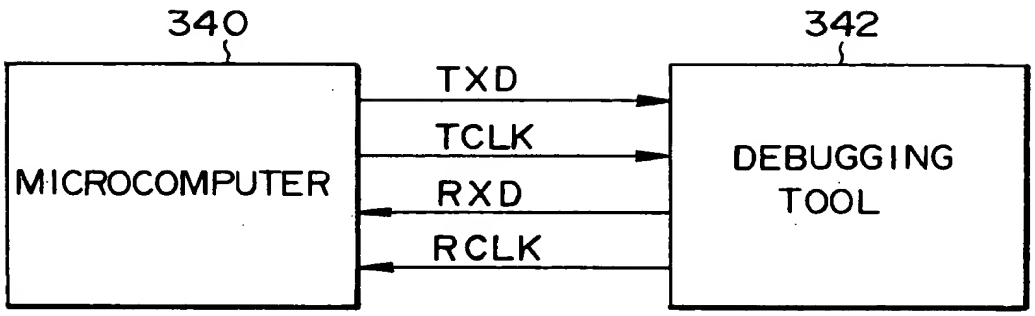


FIG. 14B

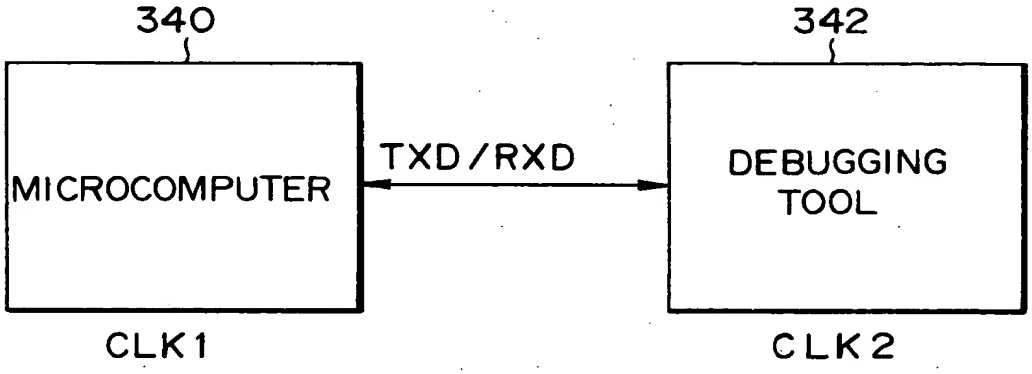


FIG. 15A

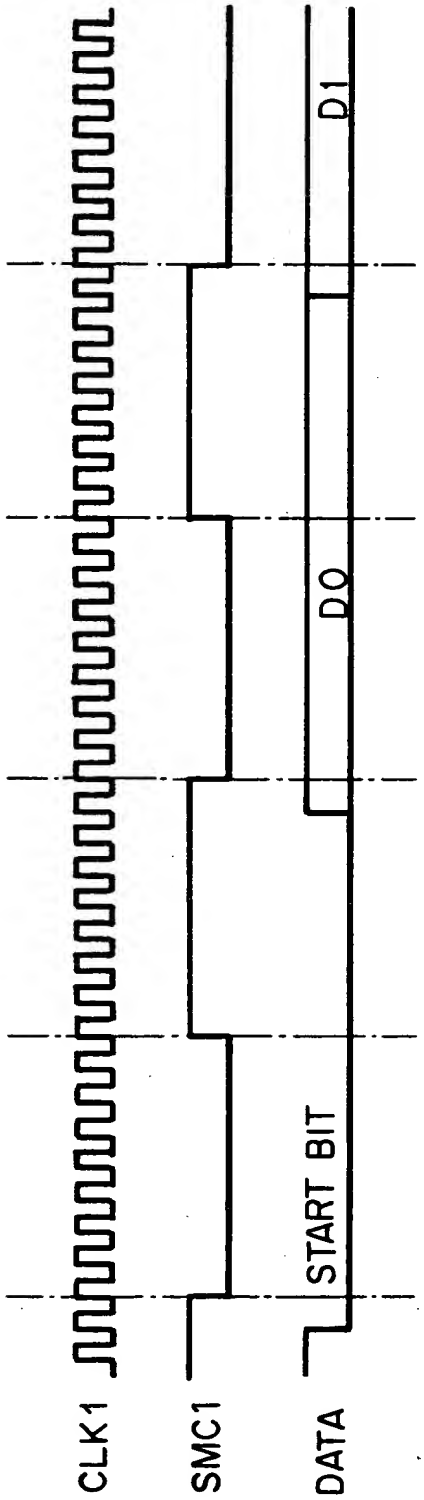


FIG. 15B

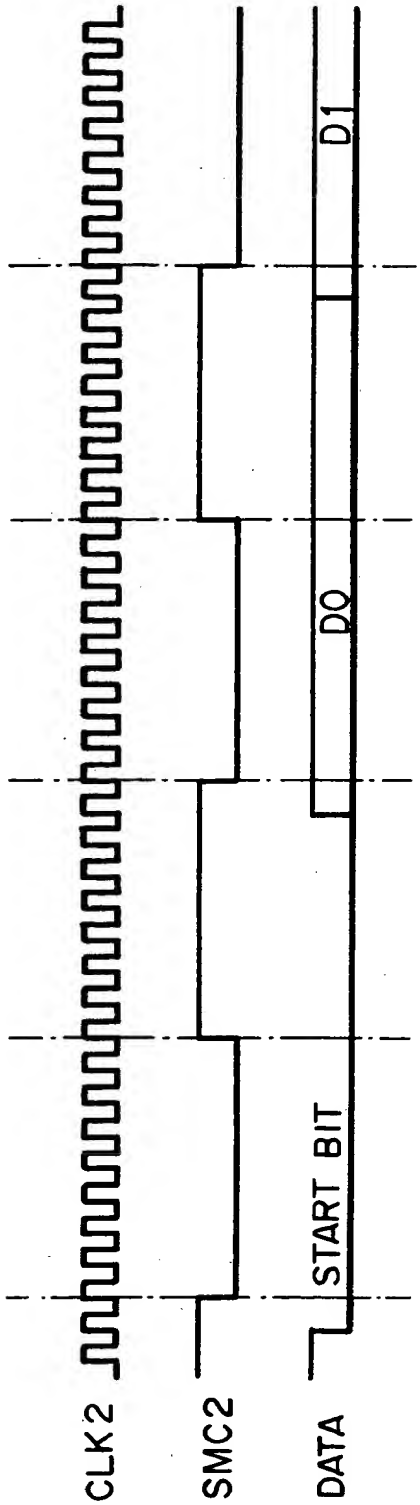


FIG. 16

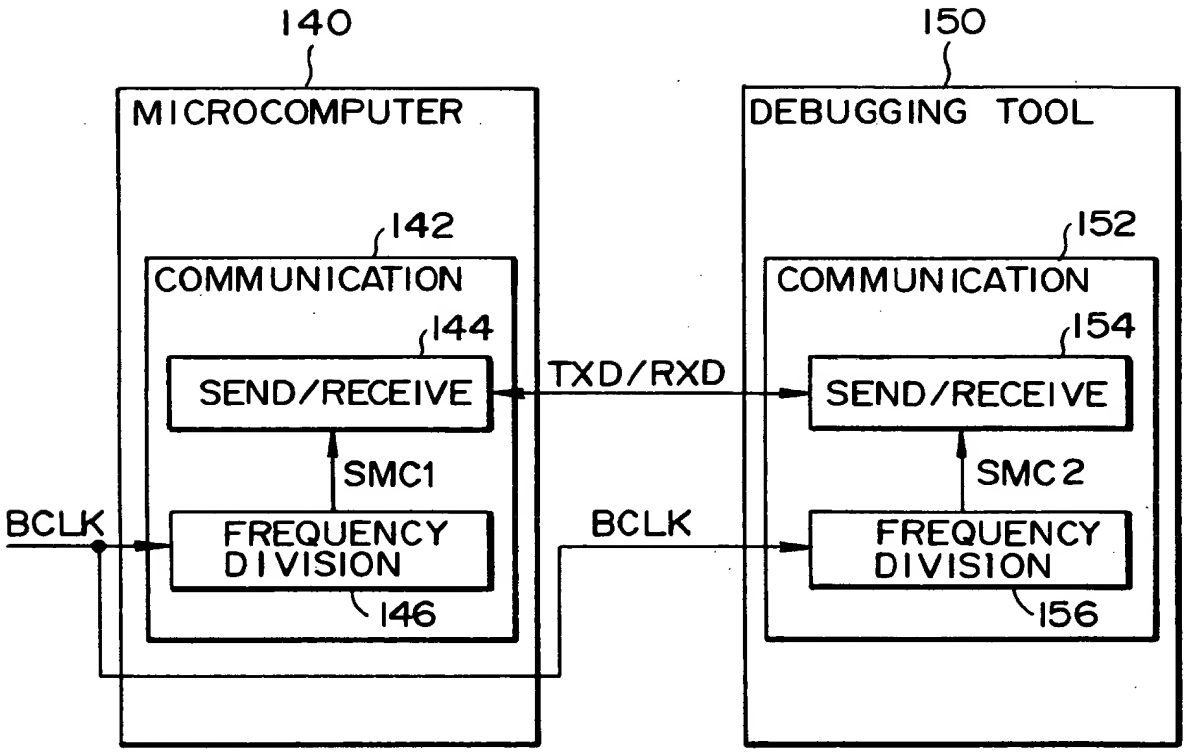

140
MICROCOMPUTER
142
COMMUNICATION
144
SEND/RECEIVE
SMC1
BCLK
FREQUENCY DIVISION
146
TXD/RXD
BCLK
150
DEBUGGING TOOL
152
COMMUNICATION
154
SEND/RECEIVE
SMC2
FREQUENCY DIVISION
156

FIG. 17A

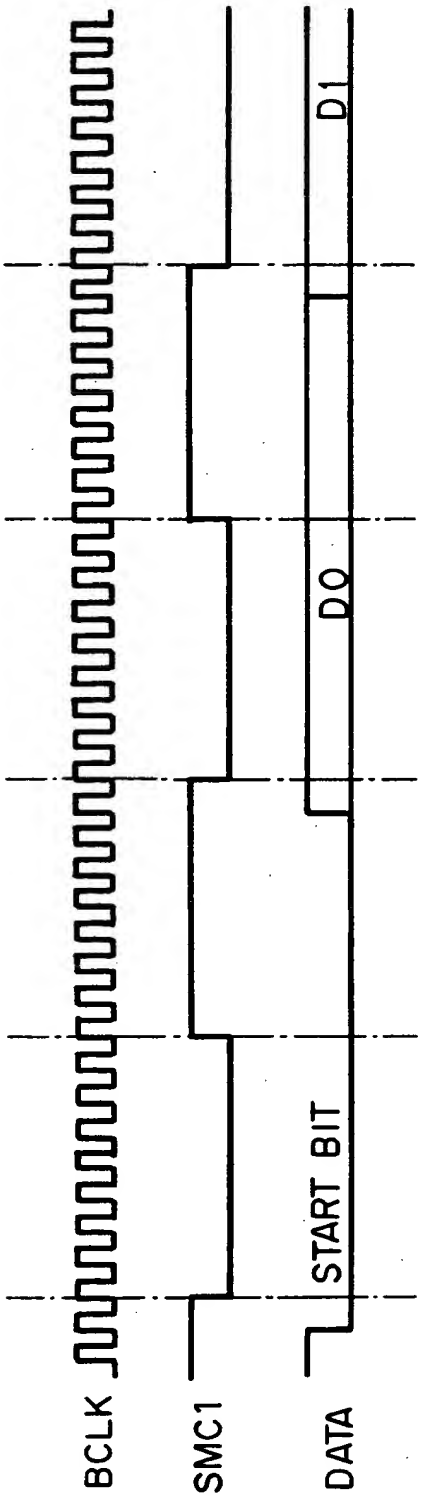


FIG. 17B

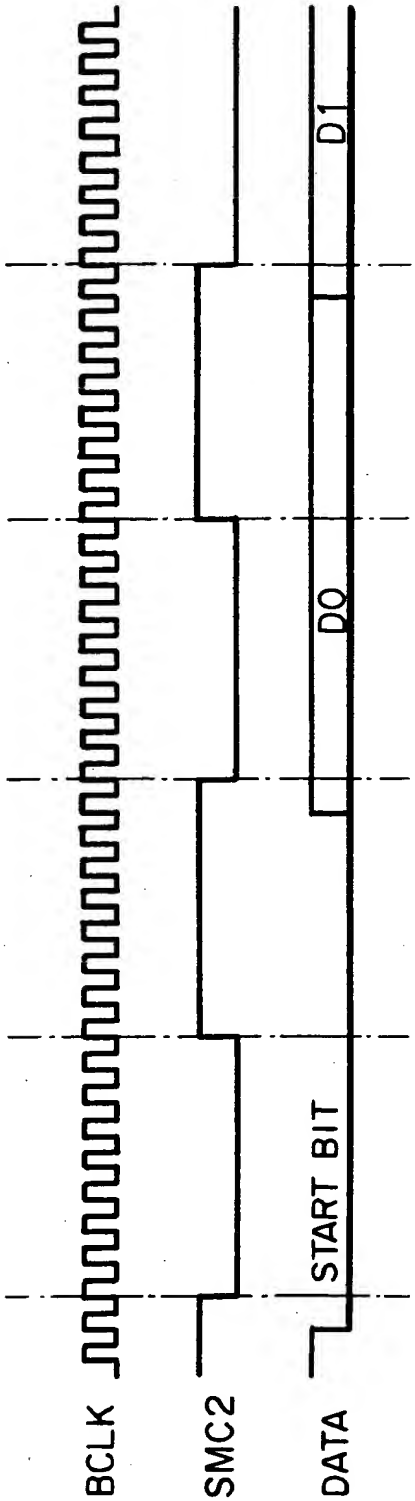
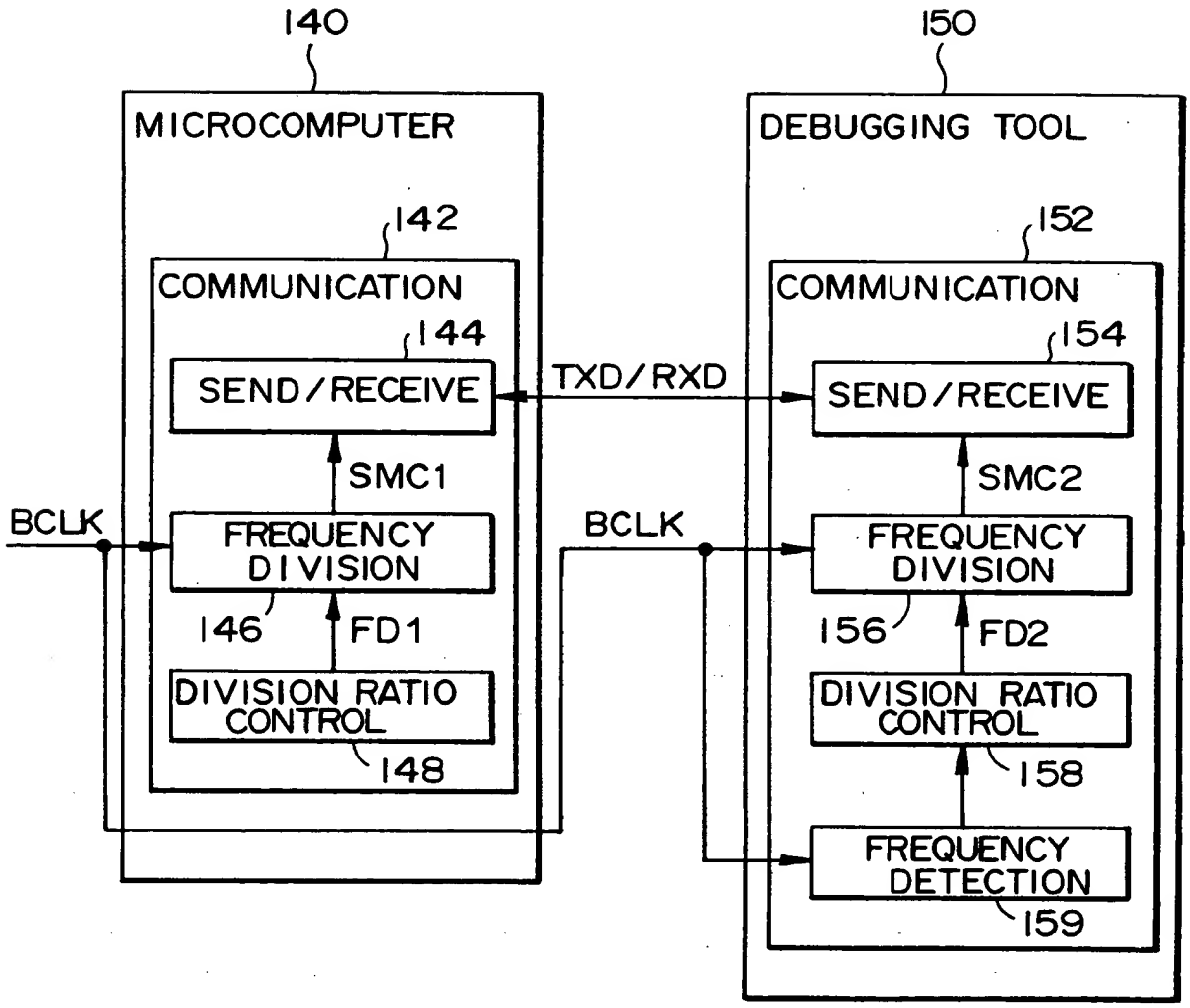


FIG. 18


140
MICROCOMPUTER
142
COMMUNICATION
144
SEND/RECEIVE
SMC1
BCLK
FREQUENCY DIVISION
146
FD1
DIVISION RATIO CONTROL
148
TXD/RXD
150
DEBUGGING TOOL
152
COMMUNICATION
154
SEND/RECEIVE
SMC2
BCLK
FREQUENCY DIVISION
156
FD2
DIVISION RATIO CONTROL
158
FREQUENCY DETECTION
159

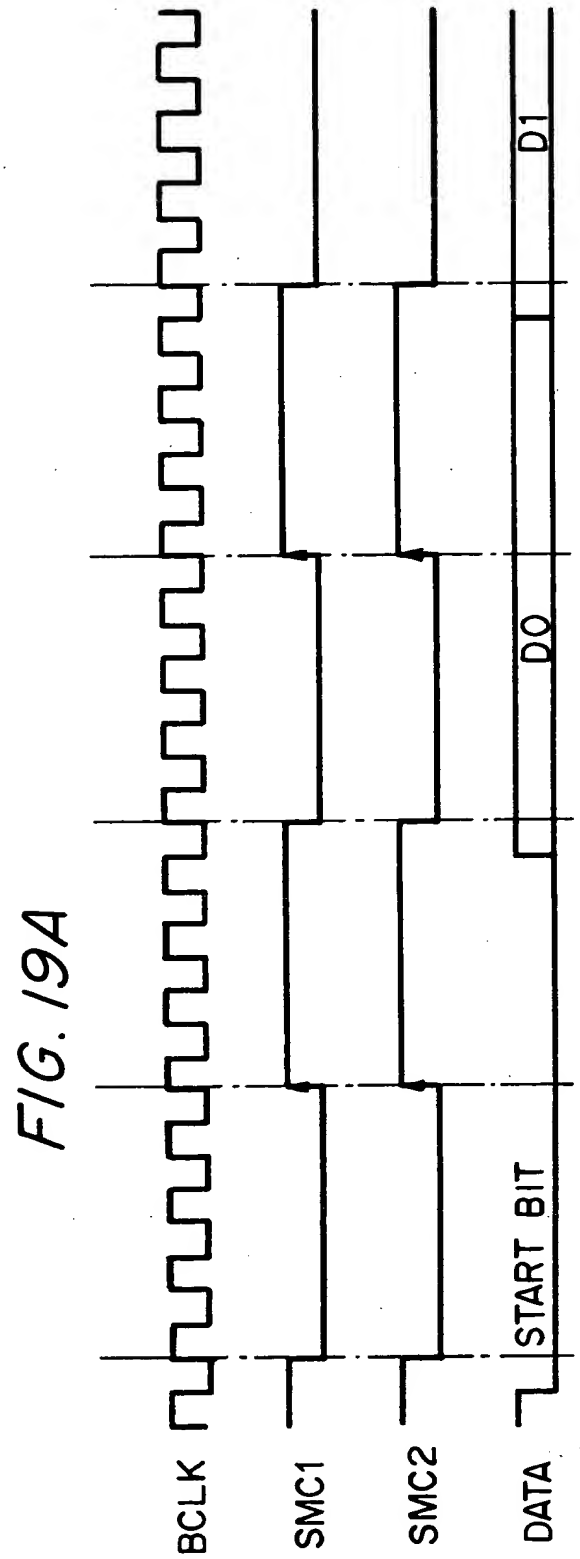


FIG. 19A

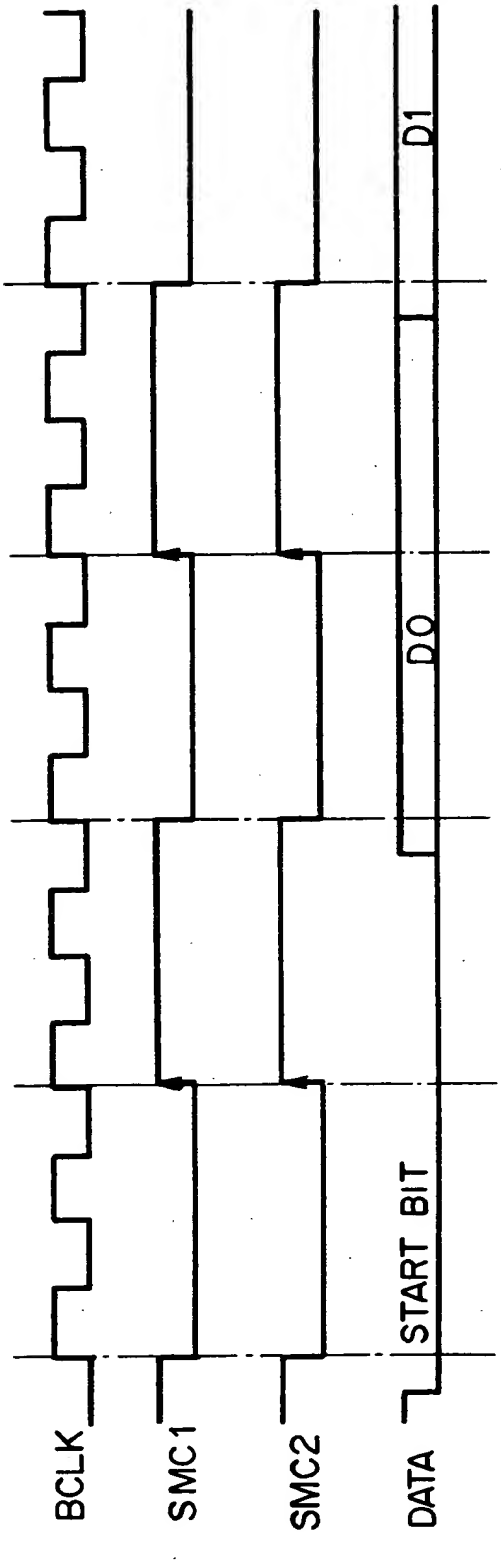


FIG. 19B

FIG. 20

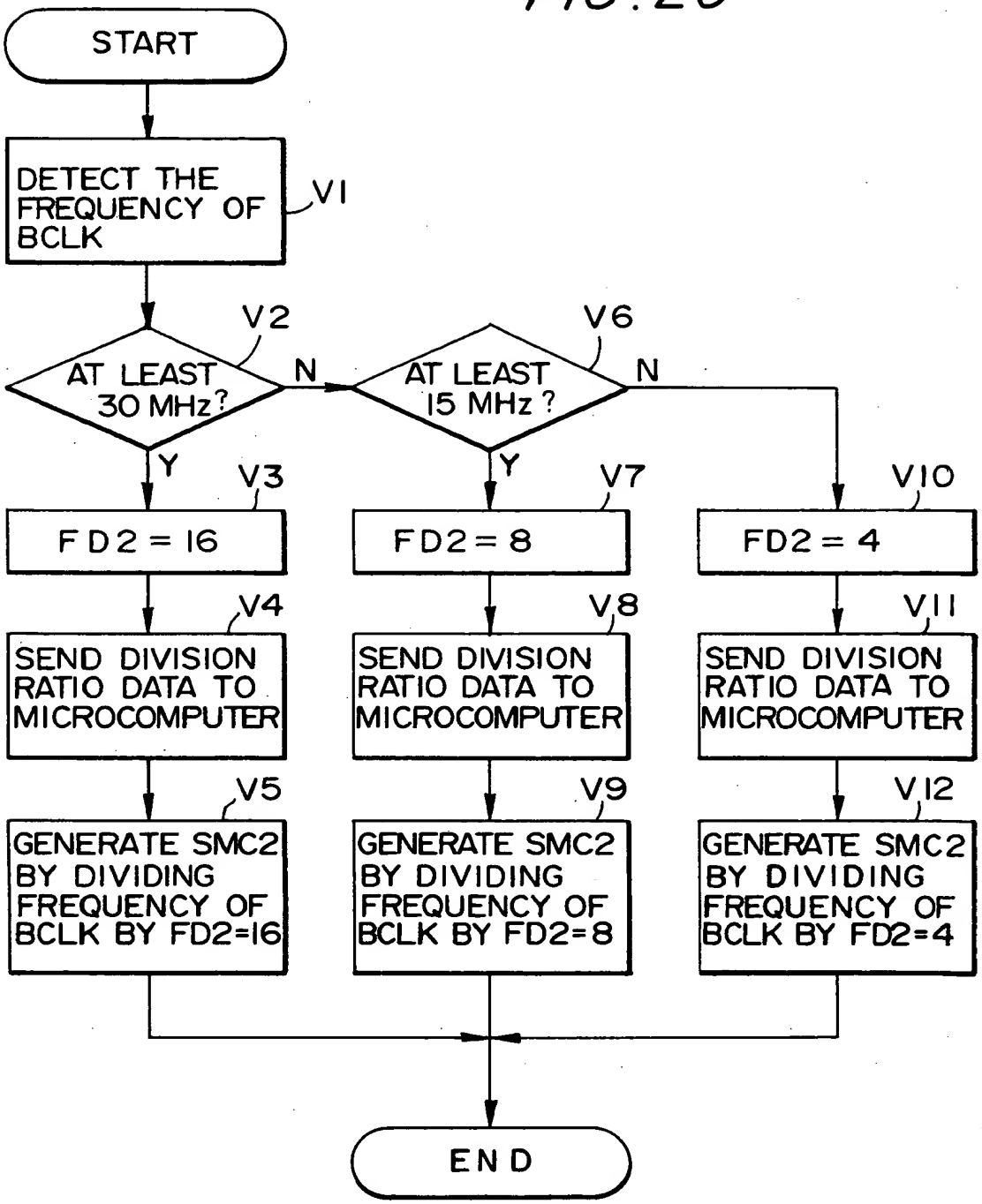

START
DETECT THE FREQUENCY OF BCLK
V1
V2
AT LEAST 30 MHz?
N
Y
V6
AT LEAST 15 MHz ?
N
Y
V3
FD2 = 16
V7
FD2 = 8
V10
FD2 = 4
V4
SEND DIVISION RATIO DATA TO MICROCOMPUTER
V8
SEND DIVISION RATIO DATA TO MICROCOMPUTER
V11
SEND DIVISION RATIO DATA TO MICROCOMPUTER
V5
GENERATE SMC2 BY DIVIDING FREQUENCY OF BCLK BY FD2=16
V9
GENERATE SMC2 BY DIVIDING FREQUENCY OF BCLK BY FD2=8
V12
GENERATE SMC2 BY DIVIDING FREQUENCY OF BCLK BY FD2=4
END

FIG. 21

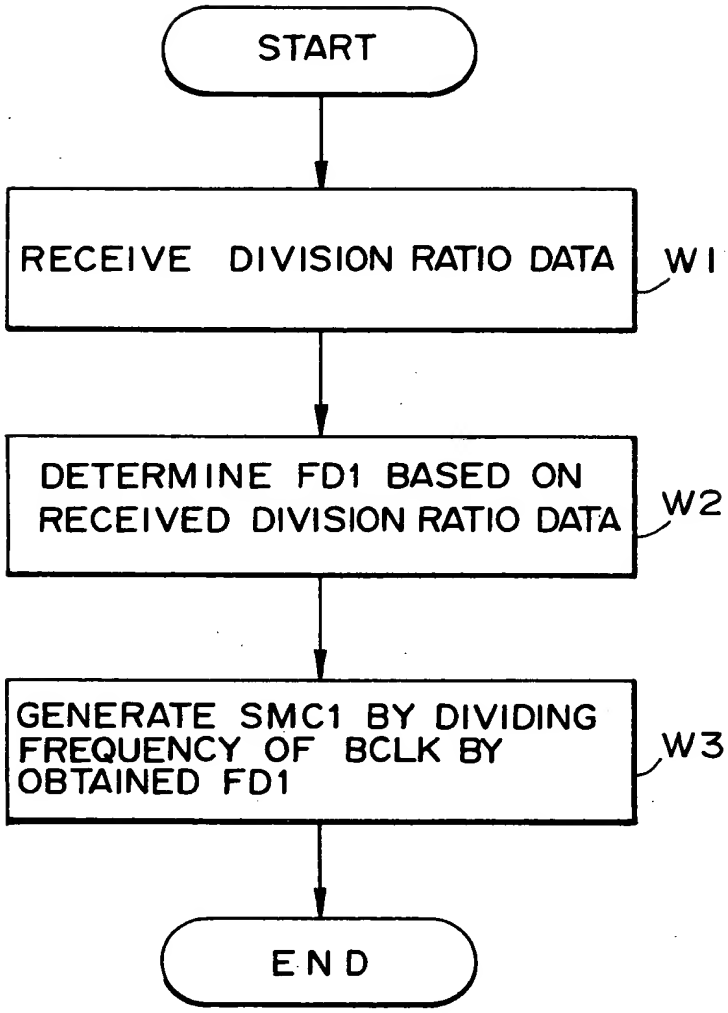

START
RECEIVE DIVISION RATIO DATA
W1
DETERMINE FD1 BASED ON RECEIVED DIVISION RATIO DATA
W2
GENERATE SMC1 BY DIVIDING FREQUENCY OF BCLK BY OBTAINED FD1
W3
END

FIG. 22

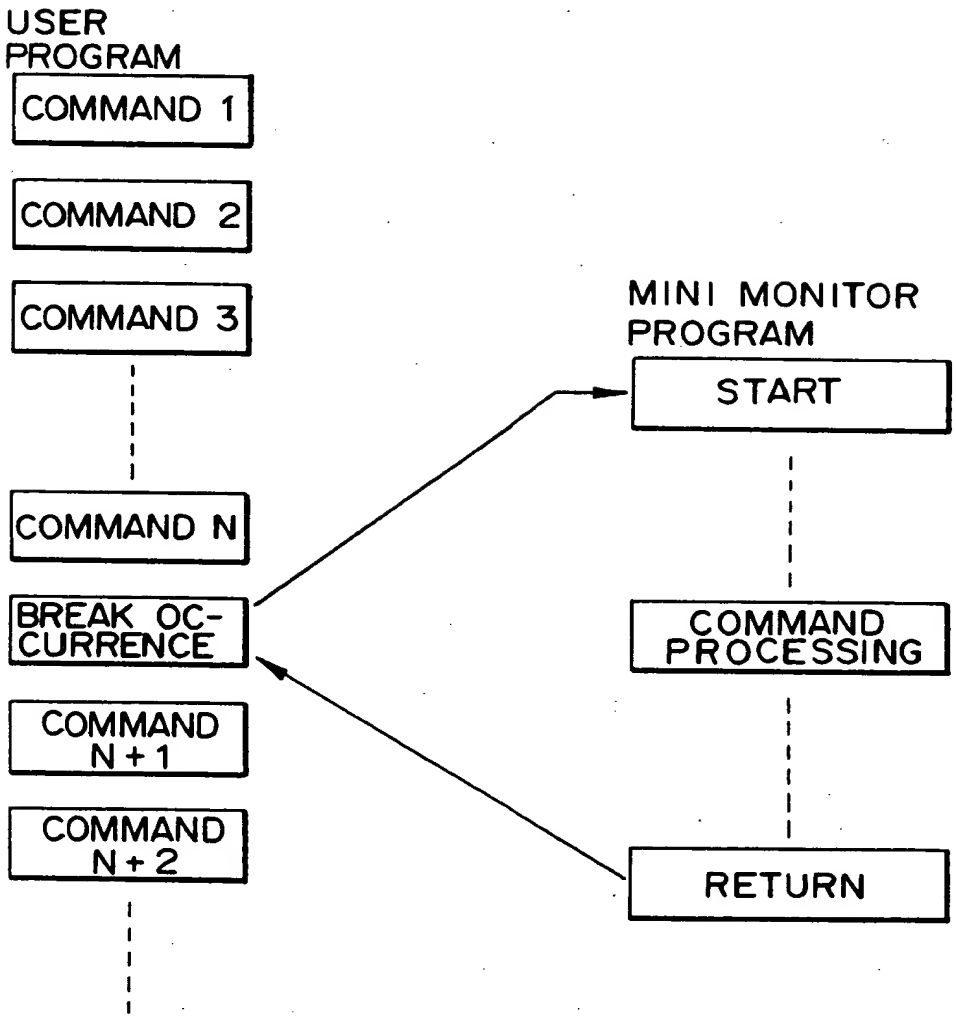

USER PROGRAM
COMMAND 1
COMMAND 2
COMMAND 3
COMMAND N
BREAK OC-CURRENCE
COMMAND N+1
COMMAND N+2
MINI MONITOR PROGRAM
START
COMMAND PROCESSING
RETURN

FIG. 23

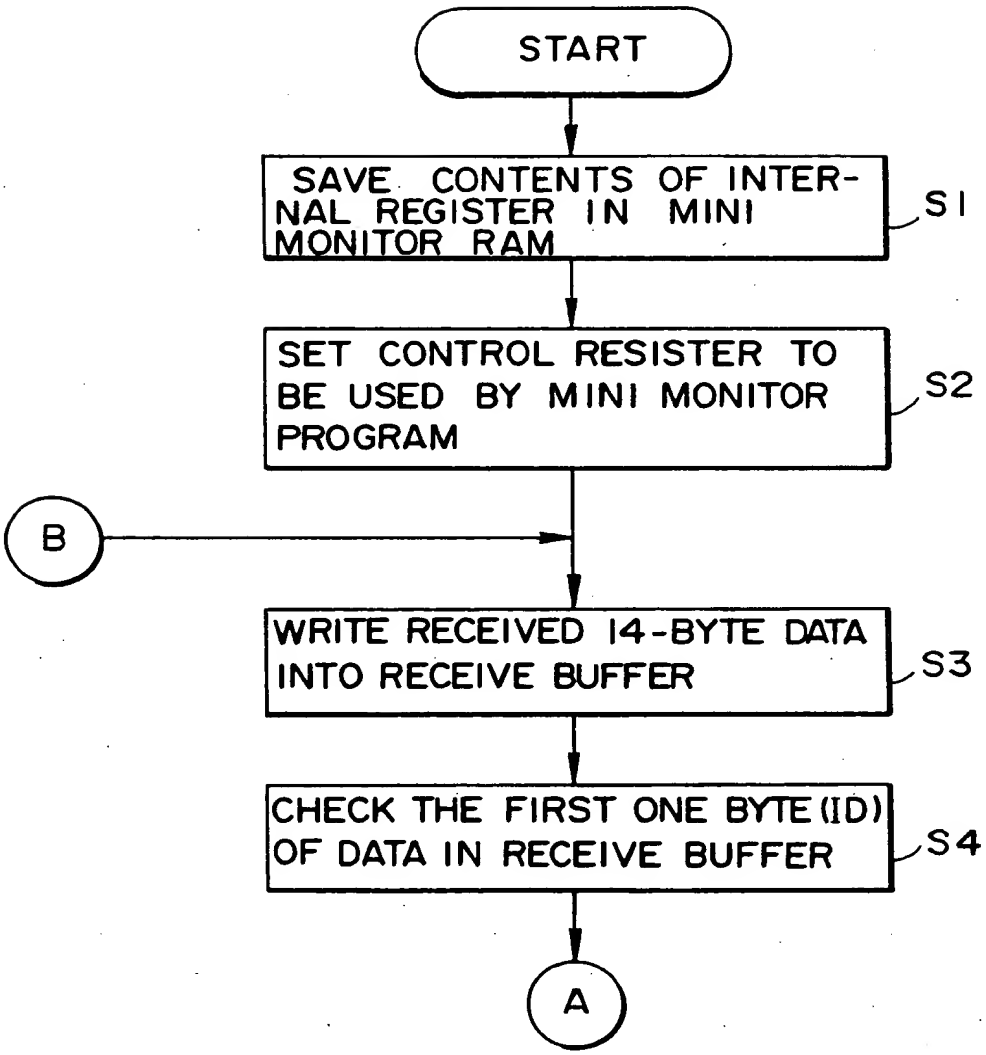

START
SAVE CONTENTS OF INTERNAL REGISTER IN MINI MONITOR RAM
S1
SET CONTROL RESISTER TO BE USED BY MINI MONITOR PROGRAM
S2
B
WRITE RECEIVED 14-BYTE DATA INTO RECEIVE BUFFER
S3
CHECK THE FIRST ONE BYTE (ID) OF DATA IN RECEIVE BUFFER
S4
A

FIG. 24

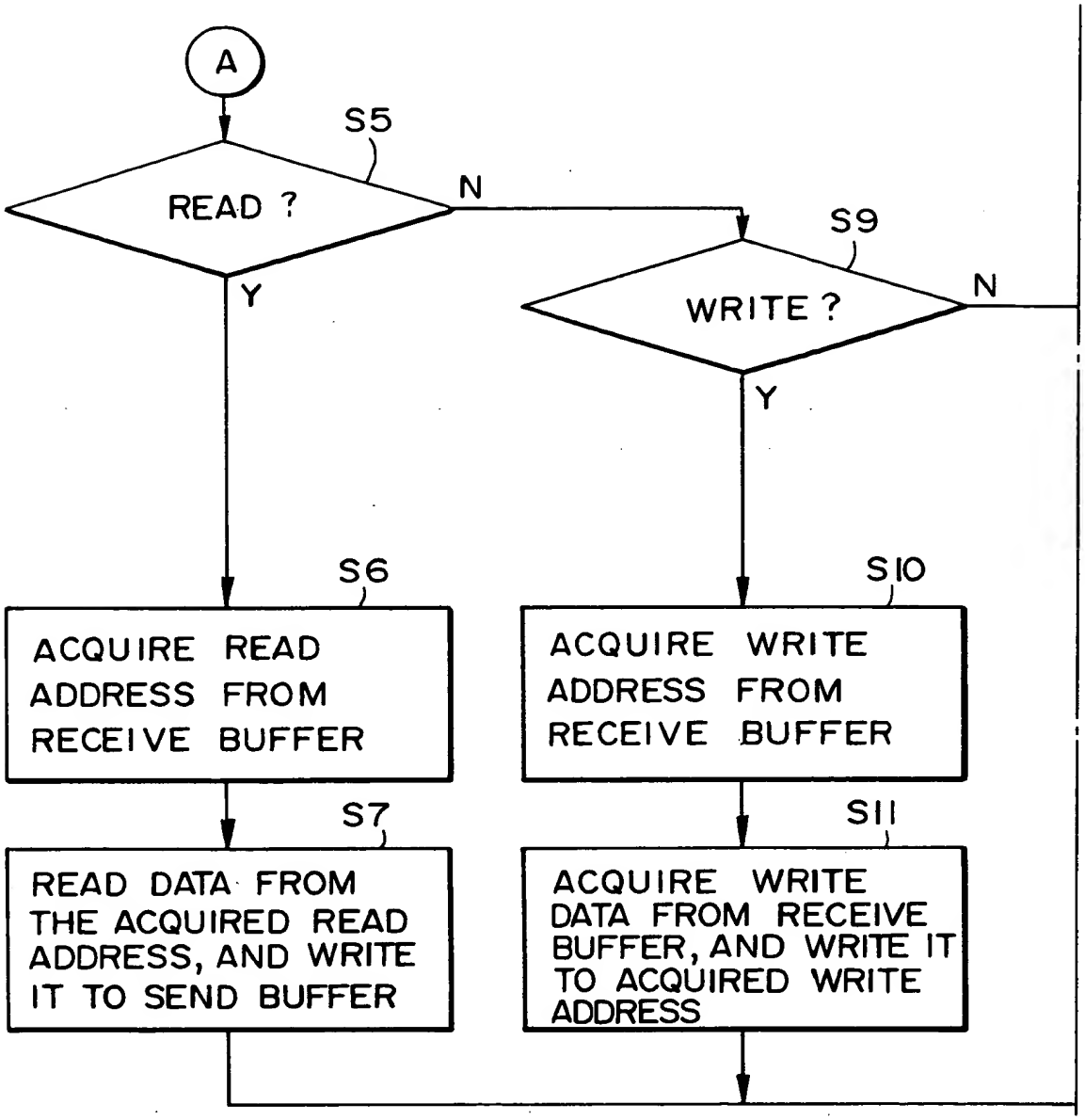

A
S5
READ ?
N
Y
S9
WRITE ?
N
Y
S6
ACQUIRE READ ADDRESS FROM RECEIVE BUFFER
S7
READ DATA FROM THE ACQUIRED READ ADDRESS, AND WRITE IT TO SEND BUFFER
S10
ACQUIRE WRITE ADDRESS FROM RECEIVE BUFFER
S11
ACQUIRE WRITE DATA FROM RECEIVE BUFFER, AND WRITE IT TO ACQUIRED WRITE ADDRESS

FIG. 24 (con't)

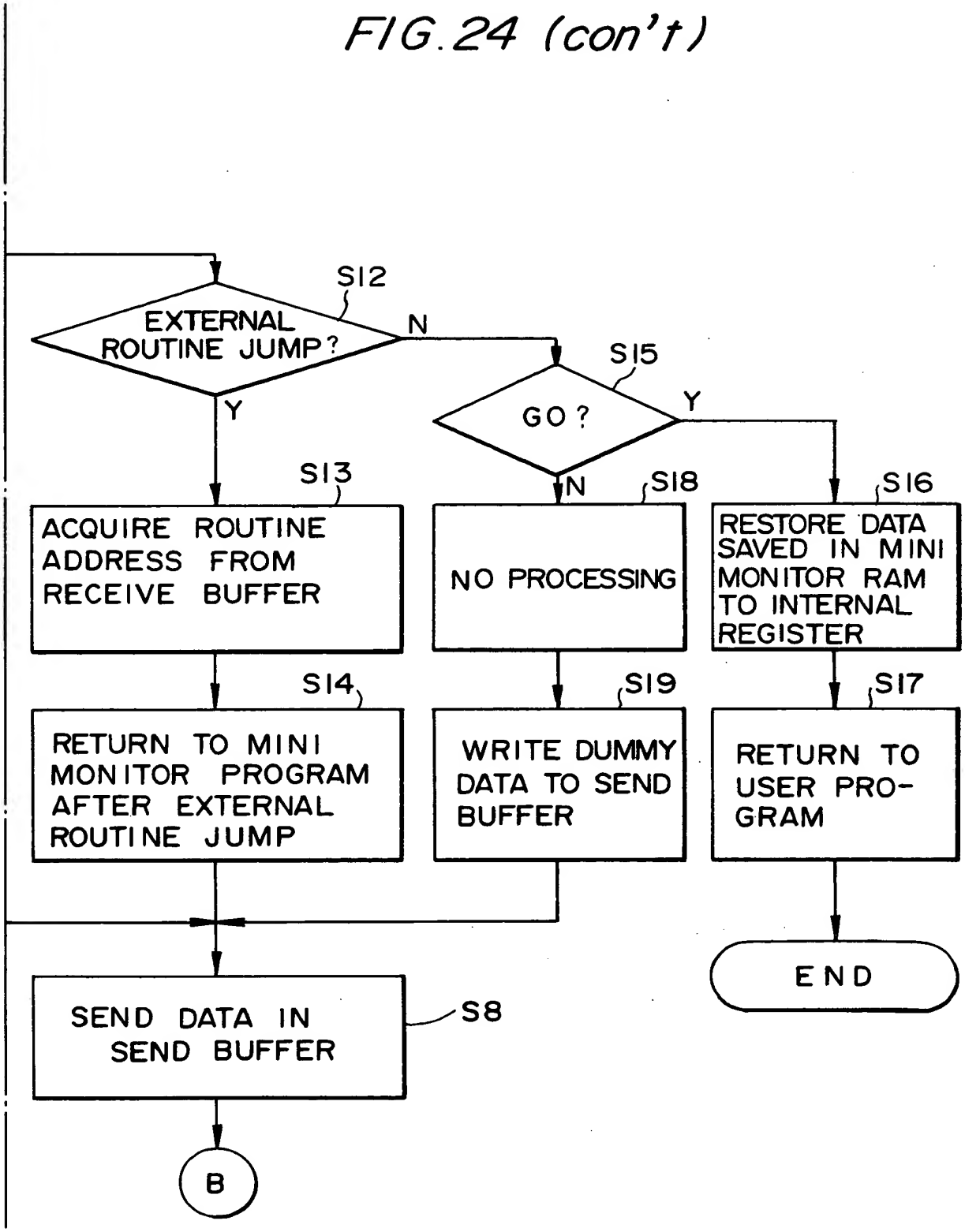

S12
EXTERNAL ROUTINE JUMP?
N
Y
S15
GO ?
Y
N
S13
ACQUIRE ROUTINE ADDRESS FROM RECEIVE BUFFER
S18
NO PROCESSING
S16
RESTORE DATA SAVED IN MINI MONITOR RAM TO INTERNAL REGISTER
S14
RETURN TO MINI MONITOR PROGRAM AFTER EXTERNAL ROUTINE JUMP
S19
WRITE DUMMY DATA TO SEND BUFFER
S17
RETURN TO USER PROGRAM
END
SEND DATA IN SEND BUFFER
S8
B

FIG. 25A

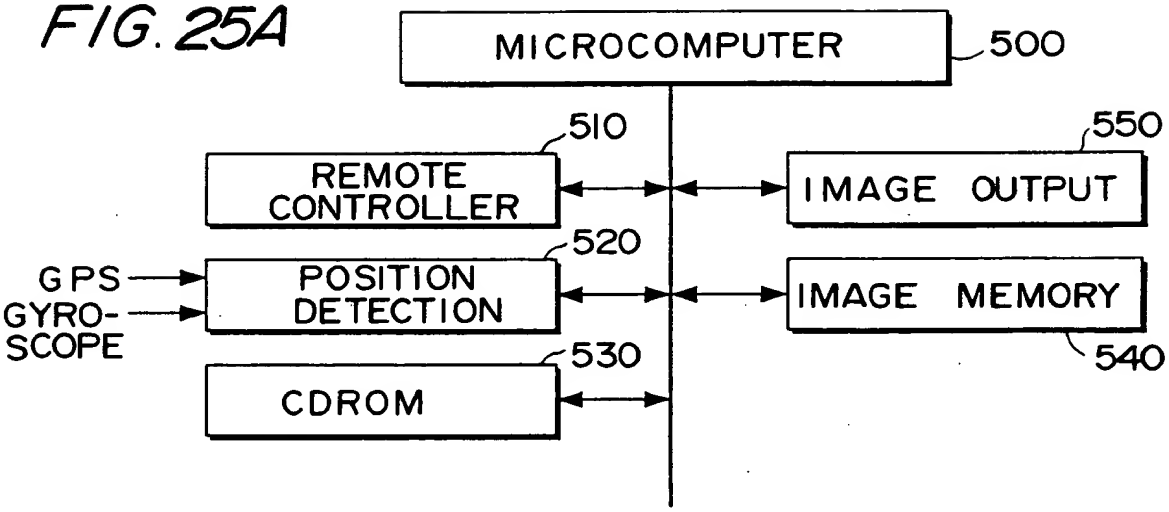


FIG. 25B

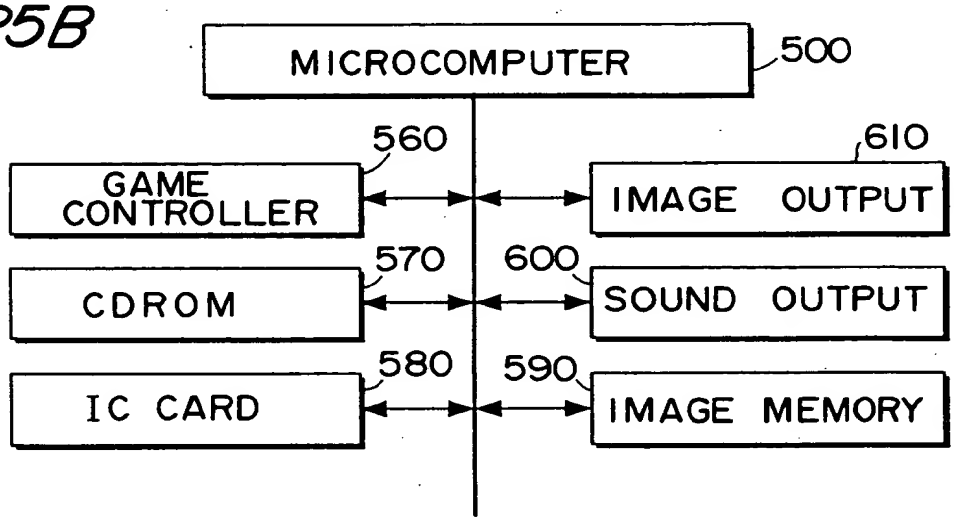


FIG. 25C

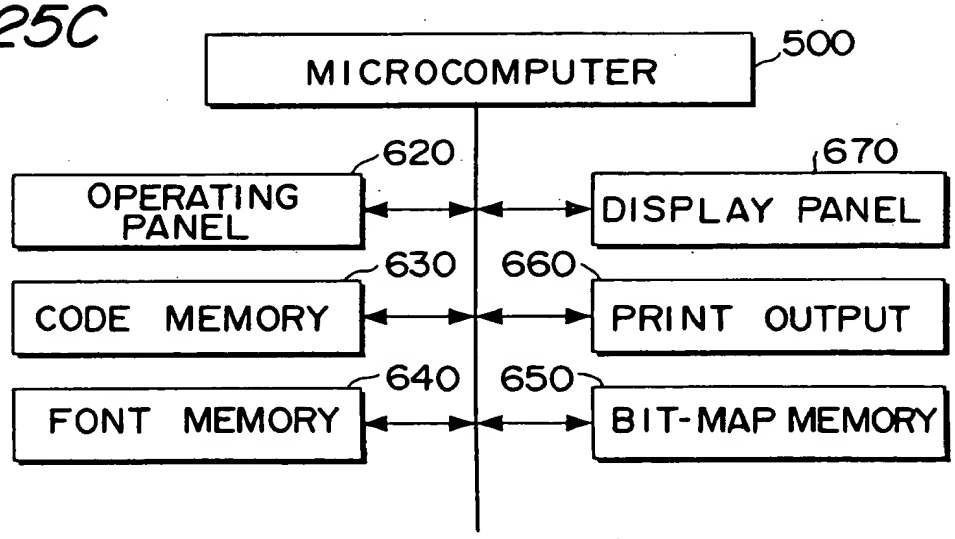


FIG.26A

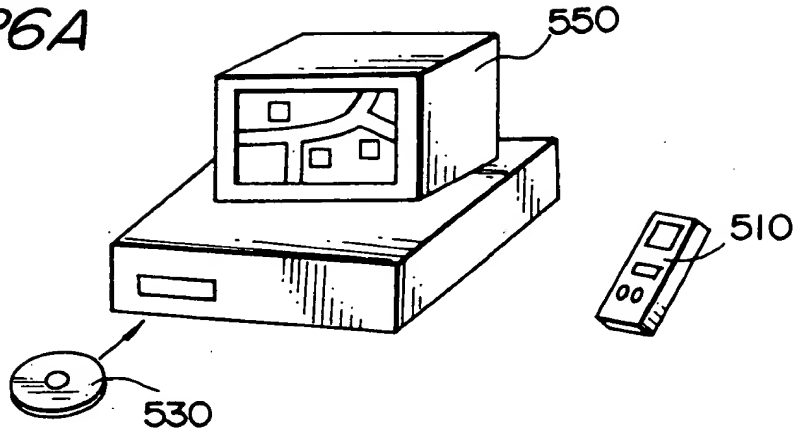


FIG.26B

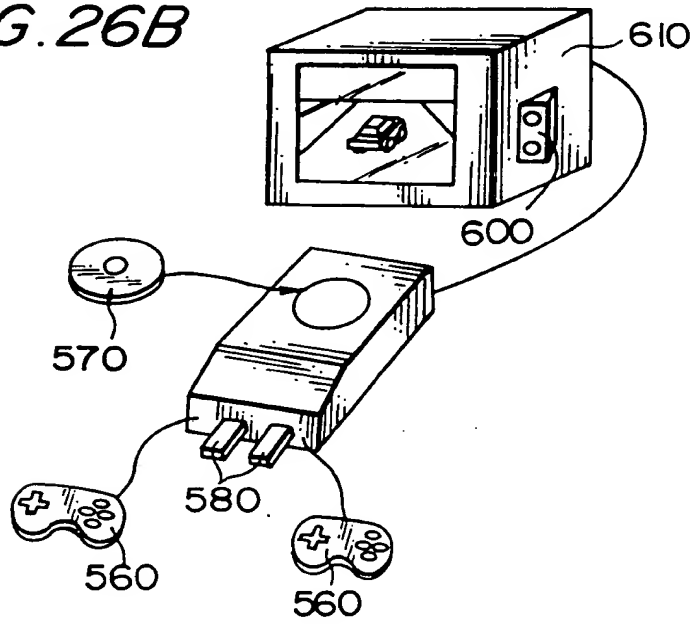
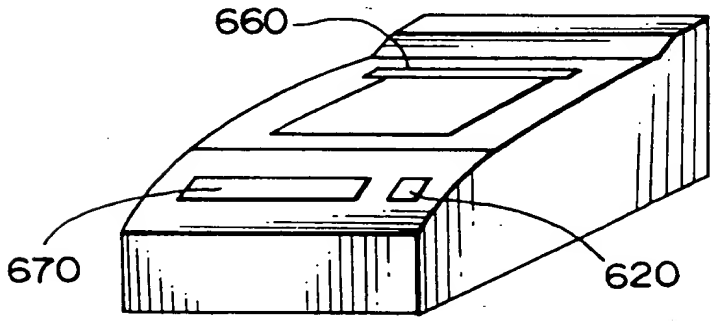



FIG.26C